WHAT IS CLAIMED IS:

1. A dual damascene interconnect structure, comprising:

a patterned multilayer of dielectrics on a substrate, comprising:

a cap layer;

a first non-porous via level low-k dielectric layer having thereon metal via conductors with a bottom portion and sidewalls;

an etch stop layer;

a first porous low-k line level dielectric layer having thereon metal line conductors with a bottom portion and sidewalls;

a polish stop layer over said first porous low-k dielectric;

a second thin non-porous low-k dielectric layer for coating and planarizing the line and via sidewalls; and

a liner material between said metal via and line conductors and said dielectric layers.

2. The dual damascene structure of claim 1, wherein said porous and said first non-porous low-k dielectric layers form covalent bonds with said etch stop layer.

3. The dual damascene structure of claim 1, wherein said first non-porous low-k dielectric layer has a material that is covalently bound to said etch stop layer.

4. The dual damascene structure of claim 3, wherein said covalently bound material is selected from the group consisting of: SiLK™, GX-3™, organic material and a combination thereof.

5. The dual damascene structure of claim 1, wherein said first porous low-k dielectric layer has a material that is covalently bound to said etchstop layer.

6. The dual damascene structure of claim 1, wherein said first porous low-k dielectric layer has a material selected from the group consisting of: porous SiLK™, porous GX-3p™, porous organic material and a combination thereof.

7. The dual damascene structure of claim 1, wherein said first porous low k dielectric material has pores with a pore size greater than 2 nm.

8. The dual damascene interconnect structure of claim 1, wherein said first non-porous low k dielectric and said first porous low k dielectric layers have identical chemical compositions.

9. The dual damascene interconnect structure of claim 1, wherein said first non-porous low k dielectric layer, said first porous low k dielectric and said second thin non-porous low k dielectric layer are organic.

10. The dual damascene interconnect structure of claim 1, wherein said etch stop layer and said second thin non-porous low k dielectric layer are silicon containing.

11. The dual damascene interconnect structure of claim 1, wherein said etch stop layer is silicon containing.

12. The dual damascene interconnect structure of claim 1, wherein said second thin non-porous low-k dielectric layer and said first non-porous low-k dielectric layer have identical compositions.

13. The dual damascene interconnect structure of claim 1, wherein said second thin non-porous low-k dielectric layer has the same chemical composition as said etch stop layer.

14. The dual damascene interconnect structure of claim 1, wherein said second thin non-porous dielectric layer has a thickness of about 20 Å to about 100 Å.

15. The dual damascene interconnect structure of claim 1, wherein said second thin non-porous low-k dielectric layer has a composition that will covalently bond with said first non-porous low-k dielectric layer and said first porous low-k dielectric layer for enhanced adhesion.

16. The dual damascene interconnect structure of claim 1, wherein said second thin non-porous low-k dielectric layer is selected from the group consisting of: HOSP™, HOSP BESt™, Ensemble™ Etch Stop, Ensemble™ Hard Mask, AP 6000™, organo silsesquioxanes, hydrido silsesquioxanes, hydrido-organo silsesquioxanes, siloxanes, silicon carbides, silicon oxides, SiLK™, GX-3™ and a combination thereof.

17. The dual damascene interconnect structure of claim 1, wherein said second thin non-porous low-k dielectric layer conformally coats the line and via sidewalls.

18. The dual damascene interconnect structure of claim 1, wherein said porous low-k dielectric layer has a thickness of about 600 Å to about 5000 Å.

19. The dual damascene interconnect structure of claim 1, wherein said etch stop layer has a chemical composition comprising silicon, carbon, oxygen and hydrogen.

20. The dual damascene interconnect structure of claim 1, wherein said etch stop layer is comprised of a spin-on material with etch selectivity to said porous low-k dielectric.

21. The dual damascene interconnect structure of claim 1, wherein said etch stop layer is selected from the group consisting of: HOSP™, HOSP BESt™, Ensemble™ Etch Stop, Ensemble™ Hard Mask, AP 6000™, organo silsesquioxanes, hydrido silsesquioxanes, hydrido-organo silsesquioxanes, siloxanes, silicon carbides, silicon oxides and a combination thereof.

22. The dual damascene interconnect structure of claim 1, wherein said etch stop layer has a thickness of about 50 Å to about 600 Å.

23. The dual damascene interconnect structure of claim 1, wherein said liner material comprises one or more metals selected from the group consisting of: Ti, TiN, Ta, TaN, W, TiW, TaSiN, WN, nitrides thereof and a combination thereof.

24. The dual damascene interconnect structure of claim 1, wherein said liner material is a material deposited by sputter deposition, physical vapor deposition (PVD), chemical vapor deposition (CVD),

ionized physical vapor deposition (Ionized PVD), atomic layer deposition (ALD) and any combination thereof.

25. The dual damascene interconnect structure of claim 1, wherein said liner material is continuous and does not penetrate into said porous dielectric.

26. The dual damascene interconnect structure of claim 1, wherein said liner material has a sharp planar interface to the dielectric layers.

27. The dual damascene interconnect structure of claim 1, wherein said metal conductor is a patterned metal conductor comprising a metal selected from the group consisting of: aluminum, copper, tungsten, gold, silver and alloys thereof.

28. The dual damascene interconnect structure of claim 27, wherein at least one of said patterned metal conductors is an electrical via.

29. The dual damascene interconnect structure of claim 1, wherein at least one of said patterned metal conductors is a line connected to said via.

30. The dual damascene interconnect structure of claim 1, wherein said first non-porous low-k dielectric layer has a metal via formed therein.

31. The dual damascene interconnect structure of claim 1, wherein said first porous low-k dielectric layer has a metal line formed therein.

32. A method of forming a dual damascene interconnect structure, comprising the steps of:

(a) forming a multilayer of dielectrics on a surface of a substrate, comprising: a cap layer; a first non-porous low-k dielectric layer; an etch stop or etch smoothing layer; a porous low-k dielectric layer; and a CMP polish stop layer;

(b) producing a multilayer of dielectrics having thereon line and via profiles having a bottom portion and sidewalls;

(c) applying a second thin, non-porous low-k dielectric layer on said bottom portion and sidewalls of said line and via profiles;

(d) selectively removing said thin, non-porous dielectric layer from said bottom portion of said vias and lines;

(e) depositing a conductive liner conformally in said line and via profiles so as to cover on said bottom portion and sidewalls of said vias and lines; and

(f) depositing a conductive metal in said line and via profiles to produce said interconnect structure.

33. The method of claim 32, wherein a first non-porous dielectric layer is formed below said etch stop layer and porous dielectric layer.

34. The method of claim 32, wherein said first non-porous dielectric layer is formed to a thickness of about 600 Å to about 5000 Å.

35. The method of claim 32, wherein said first non-porous low-k dielectric layer and said porous low-k dielectric layer have identical compositions.

36. The method of claim 32, wherein said first non-porous low-k dielectric layer is comprised of a material that forms covalent bonds with said etch stop layer.

37. The method of claim 36, wherein said etchstop layer is silicon containing.

38. The method of claim 32, wherein said first non-porous low-k dielectric layer is comprised of a material selected from the group consisting of: SiLK™, GX-3™, organic material and a combination thereof.

39. The method of claim 32, wherein said porous low-k dielectric layer is comprised of a material selected from the group consisting of: porous SiLK™, GX-3p™, porous organic material and a combination thereof.

40. The method of claim 39, wherein said porous low-k dielectric material has a pore size greater than about 2 nm.

41. The method of claim 32, wherein said porous low-k dielectric layer has a thickness of about 600 Å to about 5000 Å.

42. The method of claim 32, wherein said first non-porous low-k dielectric layer and said porous low-k dielectric layer have identical compositions.

43. The method of claim 32, wherein said first non-porous low-k dielectric layer and said porous dielectric layer have same thickness.

44. The method of claim 32, wherein said etch stop layer is a spin-on material with etch selectivity to said porous low-k dielectric.

45. The method of claim 32, wherein said etch stop layer is selected from the group consisting of: HOSP™, HOSP BESt™,

Ensemble™ Etch Stop, Ensemble™ Hard Mask, AP 6000™, organo silsesquioxanes, hydrido silsesquioxanes, hydrido-organo silsesquioxanes, siloxanes, silicon carbides, silicon oxides and a combination thereof.

46. The method of claim 32, wherein said etch stop layer comprises silicon, oxygen, carbon and hydrogen.

47. The method of claim 32, wherein said etch stop layer has a thickness of about 50 Å to about 600 Å.

48. The method of claim 32, wherein said multilayer dielectric is applied to said substrate by spin coating.

49. The method of claim 48, further comprising the step of:
curing said multilayer dielectric.

50. The method of claim 49, wherein said curing of said multilayer dielectric is a furnace curing process that is carried out at a temperature from about 300°C to about 450°C for a period of time from about 15 minutes to about 3 hours.

51. The method of claim 32, further comprising the steps of:
applying a multilayer dielectric stack to said substrate; and
baking said multilayer dielectric stack; wherein said applying and baking steps are accomplished in a single spin-coat tool.

52. The method of claim 51, further comprising the steps of:
adding additional dielectric layers; and
forming dual damascene conductors in said multilayer dielectric stack.

53. The method of claim 32, wherein said substrate is a dielectric, a metal region, an adhesion promoter, a semiconductor wafer or any combination thereof.

54. The method of claim 32, wherein said second thin, non-porous dielectric layer is applied by spin coating.

55. The method of claim 32, wherein said second thin, non-porous dielectric layer is applied by Chemical Vapor deposition.

56. The method of claim 32, wherein said second thin, non-porous dielectric layer is selectively removed from the bottom of said via and line profiles by a reactive ion etch process.

57. The method of claim 56, wherein said second thin, non-porous dielectric layer is selectively removed from the bottom of said via and line profiles by a metal liner deposition or surface preclean treatment process.

58. The method of claim 32, wherein said second thin non-porous low-k dielectric layer and said first non-porous low-k dielectric layer have identical compositions.

59. The method of claim 32, wherein said second thin non-porous low-k dielectric layer has the same chemical composition as said etch stop layer.

60. The method of claim 32, wherein said second thin non-porous dielectric layer has a thickness of about 20 Å to about 100 Å.

61. The method of claim 32, wherein said second thin non-porous low-k dielectric layer has a composition that will covalently bond with said first non-porous low-k dielectric layer and said first porous low-k dielectric layer for enhanced adhesion.

62. The method of claim 32, wherein said second thin non-porous low-k dielectric layer is selected from the group consisting of: HOSP™, HOSP BESt™, Ensemble™ Etch Stop, Ensemble™ Hard Mask, AP 6000™, organo silsesquioxanes, hydrido silsesquioxanes, hydrido-organo silsesquioxanes, siloxanes, silicon carbides, silicon oxides, SiLK™, GX-3™ and a combination thereof.

63. The method of claim 32, wherein said second thin non-porous low-k dielectric layer conformally coats the line and via sidewalls.

64. The method of claim 32, wherein said liner material comprises one or more metals selected from the group consisting of: Ti, TiN, Ta, TaN, W, TiW, TaSiN, WN, nitrides thereof and a combination thereof.

65. The method of claim 32, wherein said metal conductor is a patterned metal conductor comprising a metal selected from the group consisting of: aluminum, copper, tungsten, gold, silver and alloys thereof.